AF/2878

PTO/SB/21 (04-07)
Approved for use through 09/30/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

OIPE
SEP 10 2007
PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	7

Application Number	10/628,614
Filing Date	July 28, 2003
First Named Inventor	Roger Y. B. Young, et al.
Art Unit	2878
Examiner Name	Le, Que Tan
Attorney Docket Number	03-0460

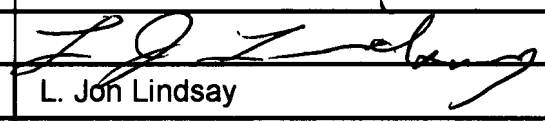
ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please Identify below):

Remarks

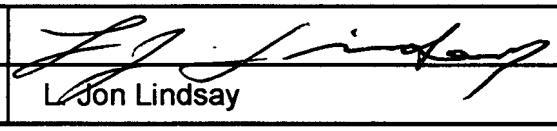
The Appeal Communication is an Amended Appeal Brief In response to the Notification of Non-Compliant Appeal Brief.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	L. Jon Lindsay, Attorney at Law		
Signature			
Printed name	L. Jon Lindsay		
Date	September 6, 2007	Reg. No.	36,855

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	L. Jon Lindsay	Date	September 6, 2007

Appl. No.	: 10/628,614	Confirmation No. 4439
Applicant	: Roger Y. B. Young, et al.	
Filed	: July 28, 2003	
TC/A.U.	: 2878	
Examiner	: Le, Que Tan	
Title	: Wafer Edge Defect Inspection Using Captured Image Analysis (as amended)	
Docket No.	: 03-0460	
Customer No.	: 024319	

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Amended Appeal Brief

Sir:

In response to the **Notification of Non-Compliant Appeal Brief** of August 8, 2007:

An **Amended Summary of claimed subject matter** begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

Amended Summary of claimed subject matter

Embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects 172-184 using captured image analysis comprising: positioning the wafer 136 with an edge thereof relative to a scanning electron microscope 132, 134 (page 10, line 24 to page 11, line 11); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the scanning electron microscope 132, 134 (page 10, lines 19-21); recording an image of the scanned wafer 136 from the scanning electron microscope 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2).

Additional embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects 172-184 using captured image analysis comprising: positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); positioning the image capturing device 132, 134 at a desired angle relative to the edge of the wafer 136 (page 12, lines 1-4); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of a desired portion of the edge of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2).

Other embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects 172-184 using captured image analysis comprising: after a first process step (e.g. at 104): positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2). after a second process step (e.g. at 106), repeating the aforementioned steps (page 5, line 27 to page 6, line 13); comparing the defect information recorded after the first process step to the defect information recorded after the second process step (page 5, line 27 to page 6, line 13); and identifying any new defects as added defects due to the second process step (page 6, line 5; page 12, line 26 to page 13, line 10).

Further embodiments of the invention include a method of inspecting a semiconductor wafer 136 for defects using captured image analysis comprising: after a first process step (e.g. at 104): positioning the wafer 136 with an edge thereof relative to an image capturing device 132, 134 (page 10, line 24 to page 11, line 11); rotating the wafer 136 (page 10, lines 19-21); scanning the edge of the rotating wafer 136 with the image capturing device 132, 134 (page 10, lines 19-21); recording an image of the scanned wafer 136 from the image capturing device 132, 134 into a database 126 (page 8, lines 19-20; page 11, lines 21-23); instructing a computer 128 to analyze the recorded images of the scanned wafer 136 (page 8, lines 27-29); identifying any defects in the analyzed recorded images (page 8, lines 29-30); and upon identifying any defects, recording defect information related to

each defect (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2). after a second process step (e.g. at 106), repeating the aforementioned steps (page 5, line 27 to page 6, line 13); comparing the defect information recorded after the first process step to the defect information recorded after the second process step (page 5, line 27 to page 6, line 13); determining whether any defects identified after the first process step have been reduced after the second process step (page 6, line 6; page 9, lines 2-3 and 27-29; page 13, lines 11-14); and identifying any such reduced defects as repaired defects (page 6, line 6; page 9, lines 2-3 and 27-29; page 13, lines 11-14).

Still other embodiments of the invention include a method of inspecting an edge of a semiconductor wafer 136 for defects during fabrication of integrated circuit components on the semiconductor wafer 136 within a fabrication system 100 that includes a plurality of fabrication stations 102-114 arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers 136 (page 5, lines 4-10), comprising: providing a plurality of inspection stations 116-122 within the fabrication system 100 corresponding to selected ones of the fabrication stations 102-114, each inspection station 116-122 being located in a subsequent processing order to a corresponding one of the selected fabrication stations 102-114 (page 5, line 10 to page 6, line 13); processing a wafer 136 in a first fabrication station (e.g. 104) (page 5, lines 11-18); automatically inspecting an edge of the wafer 136 in a first inspection station (e.g. 116) (page 12, line 26 to page 13, line 14); automatically recording a first set of defects in the edge of the wafer 136 (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2); processing the wafer 136 in a second fabrication station (e.g. 106) (page 5, lines 11-18); automatically inspecting the edge of the wafer 136 in a second inspection station (e.g. 118) (page 12, line 26 to page 13, line 14); and automatically recording a second set of defects in the edge of the wafer 136 (page 9, line 16 to page 10, line 2; page 12, line 26 to page 13, line 2).

Other embodiments of the invention include a method of inspecting an edge of semiconductor wafers 136 for defects during fabrication of integrated circuit components on the semiconductor wafers 136 within a fabrication system 100 that includes a plurality of fabrication stations 102-114 arranged in a processing order and within which a variety of process steps are performed on a plurality of wafers 136 (page 5, lines 4-10), comprising: providing a plurality of inspection stations 116-122 within the fabrication system 100 corresponding to selected ones of the fabrication stations 102-114, each inspection station 116-122 being located in a subsequent processing order to a corresponding one of the selected fabrication stations 102-114 (page 5, line 10 to page 6, line 13); processing the wafers 136 in the fabrication stations 102-114 (page 5, lines 11-18); inspecting the edge of the wafers 136 in the inspection stations 116-122 (page 12, line 26 to page 13, line 14); upon inspecting each wafer 136, recording an image of the edge of the wafer 136 (page 8, lines 19-20; page 11, lines 21-23); and correlating each recorded image with the wafer 136 from which it was taken and the process step after which it was taken (page 8, lines 20-25).

Still other embodiments of the invention include a wafer edge defect inspection system 116-122 comprising an image capturing device 132, 134, a database 126 and a computer 128 (page 8, lines 4-6). A wafer 136 can be positioned next to the image capturing device 132, 134 (page 10, line 24 to page 11, line 11). The image capturing device 132, 134 is oriented to view at least a portion of an edge of the wafer 136 (page 12, lines 1-4). The image capturing device 132, 134 automatically generates an image of the edge of the wafer 136 (page 10, lines 19-21). The database 126 is connected to the image capturing device 132, 134 to receive the generated image of the edge of the wafer 136 (page 8, lines 4-20). The database 126 automatically stores the received image for subsequent analysis (page 9, lines 5-15). The computer 128 is connected to the database 126 to retrieve the stored image upon instruction from a user to perform image analysis to locate any defects in the edge of the wafer 136 (page 8, line 27 to page 9, line 8).

Remarks

Applicant respectfully submits that the above **Amended Summary of claimed subject matter** cures the defect in the Appeal Brief filed on 11 April 2006.

Respectfully submitted,

September 6, 2007
Date

L. Jon Lindsay
Registration No. 36,855
ATTORNEY FOR APPLICANT

L. Jon Lindsay
342 Litchfield Ln.
Houston, TX 77024
Telephone: 713-984-2398
Facsimile: 928-563-4114